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Prospects and Challenges for Sub-3nm CMOS Scaling: A Critical Review of Post-FinFET Solutions

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Abstract:
FinFET technology, which offers better gate control than planar MOSFETs, enabled CMOS scaling from 22nm to 5nm. However, FinFET encounters basic electrostatic, parasitic, and manufacturing constraints that deteriorate Power-Performance-Area (PPA) scaling as the industry moves toward sub-3nm nodes. In order to control short-channel effects and replace planar MOSFET, FinFET was introduced at the 22nm node. Up to 5nm, it served as the workhorse for TSMC, Samsung, and Intel. However, FinFET encounters basic manufacturing and physical constraints when scaling gets closer to sub-3nm. This paper explores those limits and evaluates upcoming device technologies like GAA-FET and CFET that can extend Moore's Law beyond FinFET. This study examines the main drawbacks of FinFET below 3nm and compares two new device architectures. At the same time, the Synopsys Sentaurus Technology Computer-Aided Design (TCAD) simulation package is used to do the quantitative evaluation and comparative study of the FinFET and Gate-All-Around (GAA) Nanosheet FET at the 3-nm technology node.

Keywords: FinFET, Gate-All-Around, Nanosheet, CFET, Short-Channel Effects, Sub-3nm.

1. Introduction

Driven by Moore's Law for six decades [1], chipmakers have successfully scaled transistors with every new generation of technology. In order to drive the evolution of the semiconductor industry, Huawei has also suggested the "Tao (τ) Law," which is based on the idea of "time scaling" and will result in significant changes at four levels: transistors, circuits, chips, and systems [2]. To sustain the historical scaling trend, the semiconductor industry transitioned from traditional planar MOSFETs to FinFET architectures [3], which remain the modern standard. However, as scaling continues to progress, emerging short-channel effects require the development of next-generation transistor topologies. A FinFET's channel, which joins its source and drain terminals, is shaped like a fin. The gate, which provides control from all three sides, surrounds this three-dimensional channel. This multi-gate design may minimize short-channel effects, which started to degrade the transistor's performance at reduced gate lengths [4]. Planar bulk MOSFET successfully scaled to 28 nm, however below 20 nm it had severe short-channel effects (SCE), including threshold voltage fluctuation, subthreshold leakage, and drain-induced barrier lowering DIBL [5] [6]. In

2011, Intel launched FinFET at 22nm to regain electrostatic control. The gate may encircle the channel on three sides because to the 3D fin construction, which increases Cox and decreases leakage. FinFET expanded to 14 nm, 10 nm, 7 nm, and 5 nm nodes [7].

2. Literature review

Since the 1960s, according to Moore's law, metal oxide semiconductor field-effect transistors' feature sizes have been reduced to sub-micrometres and even nanometres in order to maximize the transistor density on a chip, resulting in smaller devices, quicker speeds, and lower power consumption [8]. This approach has led to the introduction of several novel materials and technologies. Fin-structured field-effect transistors, gate-all-around field-effect transistors, and 3D integration are examples of three-dimensional technologies that are being used with great effort today.

Semiconductor technology is constantly being pushed to its limits by the insatiable desire for greater processing power and superior energy efficiency in contemporary electronics, which is fuelled by revolutionary technologies like artificial intelligence and the Internet of Things [9]. Transistor technology needs to continue to scale in order to meet the demands. This scaling was successfully accomplished for many years using the planar Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

Hisamoto's and others, revolutionary study presented the idea of a three-dimensional transistor, which served as the model for the contemporary FinFET and showed noticeably enhanced short channel effects (SCE) immunity [10]. By a thin silicon "fin" from the substrate and enabling the gate to wrap around three sides of the channel, the FinFET architecture overcame the drawbacks of the planar device. Compared to its planar predecessor, this offered significantly better electrostatic control [11].

A crucial turning point reached when the industry adopted FinFETs, led by Intel at the 22 nm node, allowing for continuous performance and density scaling for more than a decade [12] [13]. FinFETs significant advantages, including reduced subthreshold swing (SS), lower leakage current, and higher on-state current for a given footprint [14]. Samsung Electronics began using the FinFET manufacturing technology with its 14nm. Samsung was the first company in the sector to manufacture 10nm FinFET transistors in large quantities in October 2016 [15].

The constraints of FinFET technology at advanced nodes have also been investigated by a number of researchers. The tri-gate design of FinFET devices is shown to be inadequate for sustaining robust electrostatic control as transistor size approach the sub-5 nm scale. This restriction results in higher leakage currents and decreased device dependability [16].

A prospective substitute for FinFET devices is the gate-all-around transistor. Because the gate electrode entirely encircles the channel in GAA topologies, short-channel effects are greatly reduced and greater electrostatic control is provided. Recent research indicates that this architecture enhances device performance by permitting lower operating voltage and higher drive current [17] .

Additionally, several GAA transistor implementations, such as nanowire and nanosheet geometries, have been studied by researchers. Whereas nanosheet transistors use stacked planar channels, nanowire

transistors use cylindrical channels encircled by the gate electrode. Research has demonstrated that, in comparison to nanowire transistors, nanosheet devices offer more driving current capability and channel width control flexibility [18].

Overall, research reveals that GAA and nanosheet transistors are the most viable topologies for future scaling, even though FinFET technology is still useful for contemporary semiconductor nodes.

3. Objectives of the study

- To analyse fundamental and process-related limitations of FinFET at sub-3nm nodes.
- To compare performance metrics of FinFET vs emerging device architectures.

This study is crucial for VLSI engineers, semiconducting material manufacturers, and research institutions. Recognizing the exact replacement device is crucial for ongoing performance improvements in artificial intelligence work, Chips for the Electric Vehicles and Mobile devices without exponential power increase.

4. Methodology

This study's qualitative comparative technique is based on a thorough analysis of earlier studies and simulation-based research. The Research Boundary includes, the primary objective is to examine the structural, electrical, and manufacturing characteristics of FinFET, GAA, and nanosheet transistor designs. In addition, this study employs a systematic approach to investigate the limitations of FinFET technology and new device architectures for sub-3nm CMOS scaling. The study comprises:

- first, **Review of FinFET and Nanosheet**: Advantages and limitation, emerging device architecture, FinFET scaling limits.
- Second is **TCAD Simulation:** Use Sentaurus tools to simulate FinFET 3nm vs Nanosheet 3nm for $I_D - V_{GS}$, $I_D - V_{DS}$, I_{Dsat}, I_{OFF} , V_{TH}.

5. review of FINFET & scaling CMOS beyond FINFETS

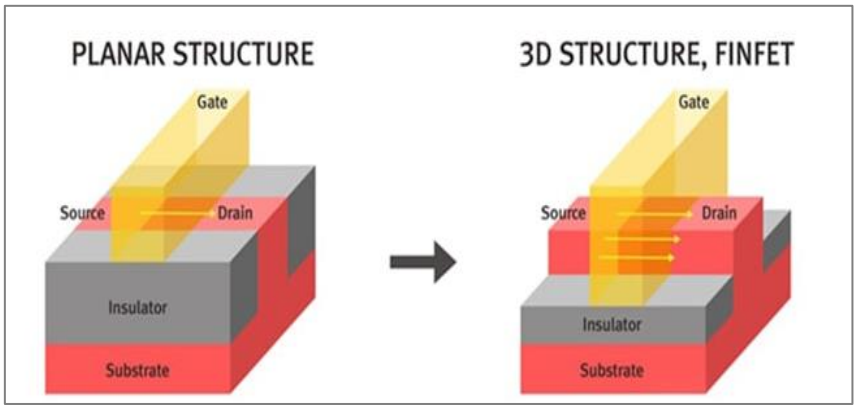
A need for continued miniaturisation of microelectronic device and improvements in processing performance has been intimately associated with the development of transistor designs [19]. The semiconductor industry's technical roadmap has traditionally been shaped by the idea of Moore's law, which states that transistor density will double roughly every two years. However, the continuation of this trend is threatened by fundamental physical limits that conventional device architectures encounter when transistor size approach atomic scales [20]. Here we will study the review of the technology from FinFET and beyond.

5.1 FinFET

"The FinFET (Fin Field Effect Transistor) process is a 3D process adopted to overcome the limitations of conventional planar (2D) structures. The structure looks like a fish's fin, hence the name 'FinFET'. In a transistor, when voltage is applied to a gate, current flows through a channel from a 'source' to a 'drain'. The broader the contact area between the gate and the channel is, the greater the efficiency is. In the FinFET process, a fin-shaped 3D structure is used to increase the contact area, thereby improving semiconductor performance and reducing leakage current [21]."

In 2012, the first 22nm FinFETs were made available for purchase [22]. Since then, FinFET architectures have been improved to decrease area and improve performance. For example, the FinFET's three-dimensional design allowed for a larger device driving current while keeping the same footprint by raising the fin height. Currently, more 10nm/7nm circuits with FinFETs "inside" are being manufactured. At the cell level of the most advanced nodes, standard cells with a track height of 6T include as few as two fins per device [23]. The most physically important change in CMOS architecture in over a decade is represented by gate-all-around nanosheet transistors, which replace the three-sided gating of FinFETs with a wrap-around gate that simultaneously controls all of the surfaces of stacked silicon nanosheets [24].

5.1.1. FinFET Structure and Operating Principle: A FinFET replaces the planar channel with a thin vertical silicon “fin”. Gate material wraps 3 sides of the fin, as shown in Figure 1.



(Image source: Planar to 3-D structure of FinFET; semiconductor.samsung.com [25])
Figure 1: Evolving architectures Planar MOSFET to FinFET

Current flows along the fin length and effective width $W_{eff} = W_{fin} + 2H_{fin}$. Where H_{fin} is fin height and W_{fin} is fin width as shown in figure 2.

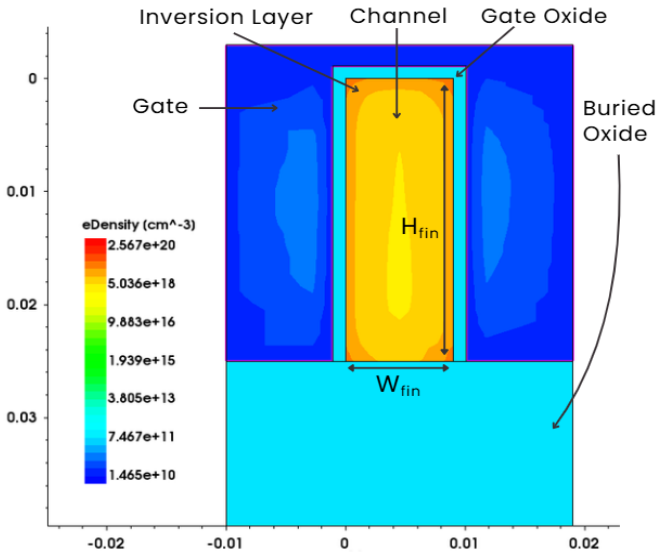


Figure 2: n-FinFET channel cross section and electron density profile

Advantages over planar: Better gate control. Second, Lower I_{OFF} due to fully depleted fin. And, Higher drive current per footprint due to 3D conduction. FinFET became industry standard at 16nm/14nm and scaled to 5nm.

5.1.2. Limitations of FinFET at Sub-3nm: Table 1 illustrates the five main restrictions that arise as scaling continues:

Table 1: Limitations of FinFET

	Parameter	description
1	Electrostatic Control Loss	Fin width cannot be scaled below ~5nm without losing gate control, and results in increased leakage, DIBL. Gate control depends on W_{fin}. When W_{fin} <5nm, the fin becomes too narrow to supply sufficient I_{ON}. Quantum confinement raises V_{TH} and reduces mobility by 30-40%. DIBL increases to >80 mV/V at 3nm vs <50 mV/V at 7nm.
2	Parasitic Resistance and Capacitance	Narrow fins increase source/drain resistance. Fin-to-fin spacing increases capacitance, limiting speed. Source/drain epi growth area shrinks with fin pitch. Contact resistance Rsd rises to 200-300 Ω-μm at 3nm, consuming 35% of total delay. Fin-to-fin capacitance also increases due to tighter spacing, hurting switching speed
3	Process Variability and Yield	Fin height/width roughness causes large V_{TH} variation. EUV + fin etch defects reduce yield below 3nm. Fintech and EUV patterning cause fin height/width roughness LWR. 1nm variation in W_{fin} results in 25mV V_{TH} shift. At 3nm, defect density and yield loss become major cost drivers.
4	Thermal and Mobility Issues	3D fin structure traps heat, worsening self-heating at high power density. Sidewall surfaces scatter carriers which lowers electron/hole mobility as compared to planar devices. Tall fins trap heat. Self-heating raises channel temperature by 30-50°C at high power, reducing mobility further. Sidewall surface scattering lowers electron mobility vs planar devices.
5	Area Scaling Limit	Cell height limited by fin pitch. Contacted gate pitch ~42nm at 5nm node is near physical limit.

Below 3nm, FinFET shows diminishing returns: <15% performance gain per node vs historical 30%.

5.2. Emerging Device Architectures: Two architectures are evolving to get around FinFET constraints, as seen in figure 3:

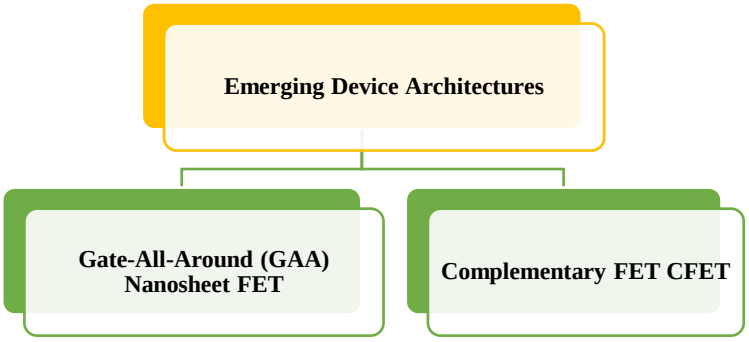
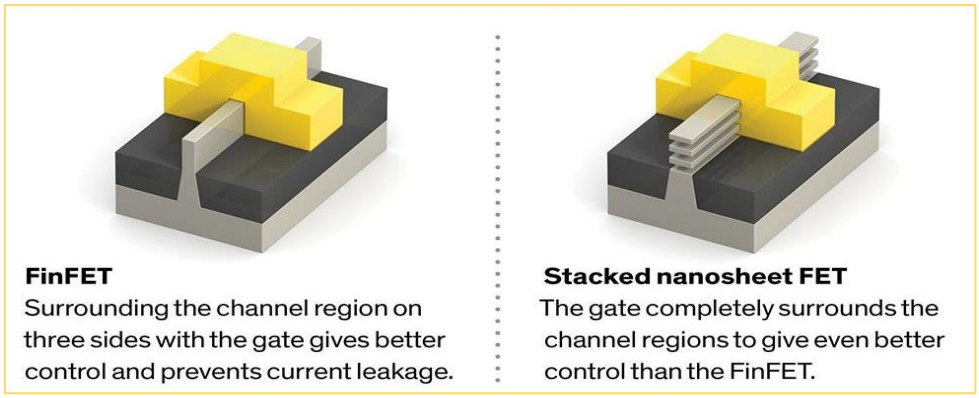


Figure 3: Evolving architectures above FinFET constraints

5.2.1: Nanosheets an Evolution of the FET

Since its development in 1959, the field-effect transistor has mostly been integrated into the silicon plane. To further control current leakage, it will now take the shape of stacked sheets instead of a projecting fin. Evolving architectures FinFET to Nanosheet FinFET is shown in figure 4.



(Image Courtey: IEE Spectrum, Evolution of the FET: [26])

Figure 4: Evolving architectures FinFET to Nanosheet FinFET

FinFETs are replaced at the 2nm node by Gate-All-Around (GAA) nanosheet transistors because the three-sided gate of FinFET can no longer stop the drain's electric field from entering the channel at gate lengths less than around 7nm, a failure mode identified as drain-induced barrier lowering (DIBL) [27]. DIBL occurs when the electric field from the drain enters the channel, lowering the threshold voltage and the source-side potential barrier [28]. The unshielded channel that would ordinarily allow the drain field to reach the source is eliminated by GAA's four-sided enclosure of each nanosheet. By simultaneously encasing each channel area with gate dielectric and gate metal on all four sides, GAA enhances gate-to-channel coupling and decreases off-state leakage at the dimensions required for 2nm-class CMOS. 2-5 horizontal silicon nanosheets stacked vertically, gate surrounds each sheet on all 4 sides. Samsung launched 3nm GAA-MBCFET in 2022 [29].

Vertically stacked nanosheets: the FinFET structure is unable to offer sufficient electrostatic control at reduced gate lengths [30]. Furthermore, even if fin height is further increased, the evolution to lower track height standard cells necessitates a switch to single-fin devices, which cannot supply sufficient driving current [31] . Vertically stacked nanosheet transistors can help in this situation. They can be viewed as the FinFET device's organic progression. Imagine putting a FinFET on its side and creating the channels by splitting it into distinct horizontal sheets. The channel is now completely encircled by a gate. Compared to the multi-gate FinFET, the nanosheet's gate-all-around design offers better channel control as effective width $W_{eff} = 2N(NS_W + NS_H)$, where NS_W is nanosheet width and NS_H is nanosheet thickness as shown in Figure 5. Simultaneously, the effective drive per footprint is optimized by the more ideal distribution of the channel cross-section in the 3D volume [32].

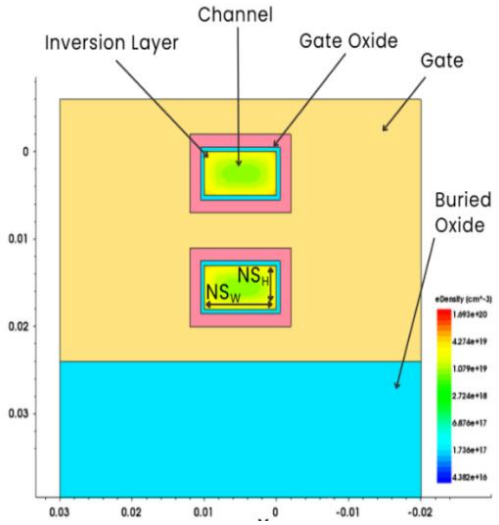
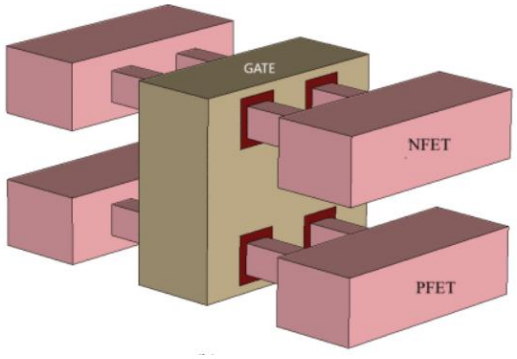


Figure 5: n-Nanosheet FET channel cross section and electron density profile

The Gate-All-Around GAA Nanosheet FET features a number of Advantages include: (1) 4-side gate control and (2) Sheet width (NS_W) tuning for Ion vs. area trade-off, which results in 20–30% greater Ion than FinFET at the same Ioff. The challenges include extra process steps, stacking alignment, and sheet release etch. In order to overcome this restriction, gate-all-around transistor designs completely enclose the channel with the gate electrode. This approach allows for further scaling of transistor size and greatly enhances electrostatic control. The ability to stack several channel sheets vertically is another benefit of nanosheet transistors. This arrangement improves driving current capabilities and expands the effective channel width.

5.2.2 Complementary FET (CFET)

The configuration of CFETs is vertically stacked. The necessary device footprint is reduced by this vertical integration, which is mostly limited by cell height rather than horizontal spacing. In comparison to traditional CMOS technologies, CFETs therefore provide the possibility for up to a twofold increase in integration density in addition to improving the effective channel width and drive current [33]. CFETs are exhibiting tremendous attention for their capacity to save active area in the vertical stacking of pFET and nFET devices (Fig. 6).



(image Source: IEEE Explore [34])
Figure 6: CEFT architectures

In CFET, an n-type FET (nFET) is stacked vertically on top of a p-type FET (pFET) within the same track in the new CFET 3D transistor architecture. The complementary FET (CFET) device is evaluated using a design-technology co-optimization (DTCO) methodology. Through a double level access, it offers a 50% structural scaling of SRAM and standard cells (SDC). The elevation dimension needs to be carefully managed in order for the proposed process flow to be manufactured [35].

At the same time, they can achieve excellent electrostatic integrity using the GAA or Fin architecture for the channel. Moreover, the vertical stacking of pFET and nFET enables simplified terminal access through internal shorting of the p/n drain contacts, facilitating further reduction in standard cell height and overall chip area [36] [37] [38]. CFET architectures can be broadly categorized as three distinctive architectures: fin-on-rectangular-fin (FORF), fin-on-trapezoidal-fin (FOTF), and fin-on-GAA-fin (FOGF), which have unique structural and performance advantages in the integration of advanced devices [39] [40]. Advantages of CFET comprises- (1) 50% reduction in conventional cell area compared to side-by-side n/p FinFET; and (2) Reduced RC delay and shorter routing. And challenges consist of: Heat extraction, alignment less than 2 nm, and a thermal budget of less than 500°C are necessary for monolithic 3D stacking [41].

The necessity of scaling boosts: At low cell track heights of 6T and 5T, where fin depopulation would reduce drive current in conventional FinFET-based cells, the migration to nanosheet devices becomes ideal. IMEC recently developed an inventive alternative architecture known as the forksheet device to increase the scalability of these devices. One may think of the forksheet as a logical progression of the nanosheet technology. The sheets are now controlled by a forked gate structure, in contrast to the nanosheet device. This is achieved by placing a dielectric wall between the p- and nMOS devices prior to gate patterning. This wall allows for a substantially closer n-to-p spacing by physically separating the p-gate trench from the n-gate trench [42] .

5.3. Evolution from MOSFET to FinFET to Nanosheet simulated on Sentaurus TCAD:
The evolution of transistor architecture from MOSFET to FinFET and now to Nanosheet represents a continuous effort to maintain Moore's Law by overcoming physical scaling limits. As gate lengths shrank, conventional planar MOSFETs suffered from severe short-channel effects and high leakage current because the gate could no longer effectively control the channel [43] [44]. To fix this, the industry

transitioned to FinFETs, which wrapped a 3D fin-shaped channel on three sides, drastically improving electrostatic control and reducing leakage. However, below the 3nm node, even FinFETs face scaling limits. This has triggered the shift to Nanosheet (GAA) transistors, where stacked horizontal channels are completely surrounded by the gate (Gate-All-Around), offering the ultimate electrostatic control, optimal power efficiency, and design flexibility [45]. Simulating this structural evolution in Synopsys Sentaurus TCAD involves a shift in transport models and mesh strategies. Structural analysis depicting evolution from SOI MOSFETs to FinFETs to Nanosheet is shown in figure 7:

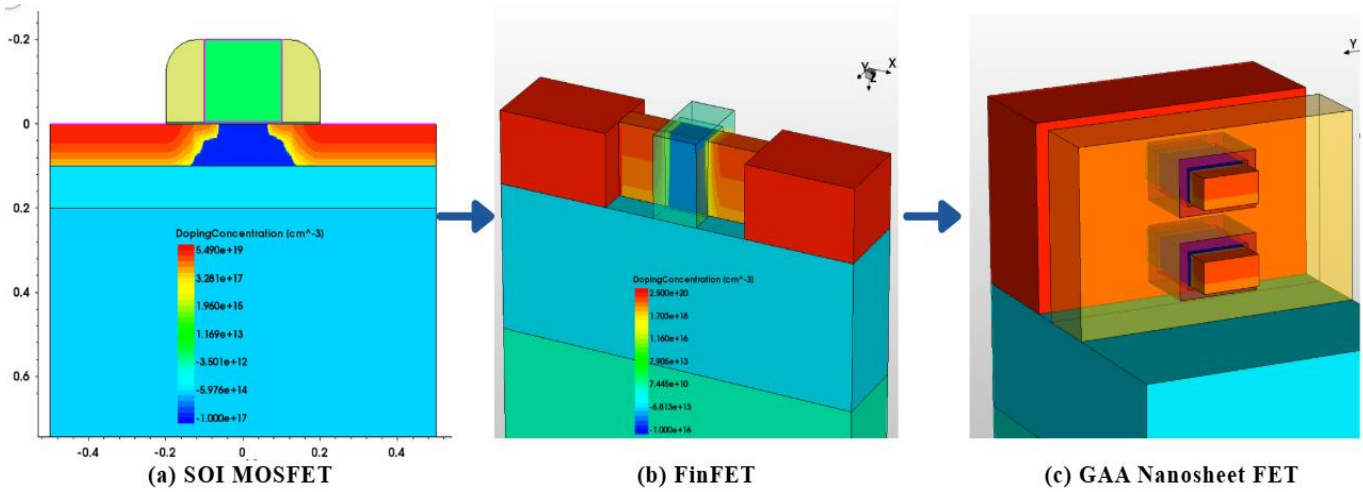
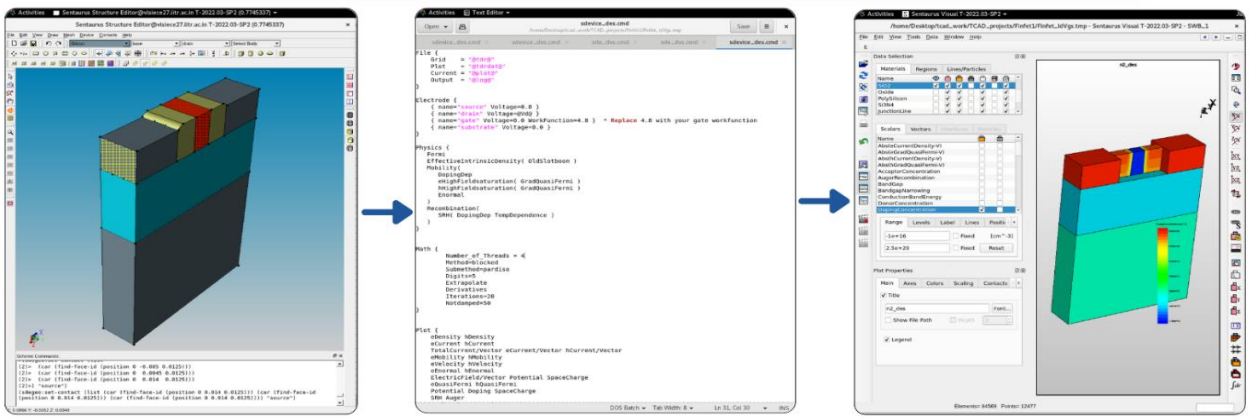


Figure 7: Structural analysis depicting evolution from SOI MOSFET to FinFET, and finally to GAA Nanosheet.

6. Methodology and Simulation Flow

The quantitative evaluation and comparative analysis of the FinFET and Gate-All-Around (GAA) Nanosheet FET at the 3-nm technology node are executed using the Synopsys Sentaurus Technology Computer-Aided Design (TCAD) simulation suite. The workflow follows a strict multi-stage process from structural discretization to multi-bias electrical extraction. Simulation workflow in Sentaurus TCAD is shown in figure 8.



(a) Sentaurus Structure Editor (SDE) (b) Sentaurus Device (SDevice) (c) Sentaurus Visual (SVisual)

Figure 8: Simulation workflow in Sentaurus TCAD

"The simulation pipeline begins in **Sentaurus Structure Editor (SDE)**, which serves as the geometric modelling engine [46]." Both architectures' precise 3D physical boundaries, oxide interfaces, material compositions, and coordinate-specific meshing profiles are specified in SDE. In order to capture high potential gradients, the structural mesh is carefully adjusted within the channel and extension zones [47].

"Once the mesh is finalized, it is compiled into the numerical solver engine, **Sentaurus Device (SDevice)**. SDevice serves as the physics core of the workflow, executing mixed-mode circuit equations and self-consistently solving coupled partial differential equations across the discrete multi-dimensional mesh grids [48]." Advanced quantum-mechanical and transport physics models are called within the SDevice command file to attain high fidelity at the 3-nm node.

Lastly, Sentaurus Visual (SVisual) receives the simulated electrical outputs and spatial distributions for post-processing. Terminal currents, electrostatic potentials, and dynamic transient capacitance profiles are extracted using SVisual, which serves as the data visualisation and analysis engine [49].

6.1 Device Structure and Doping Architecture

To ensure a rigorous and scientifically valid benchmark, both the 3-nm FinFET and the GAA Nanosheet FET are engineered with perfectly matched effective channel widths (W_{eff}).

"The structural parameters and doping landscapes are precisely controlled to replicate realistic sub-3-nm process profiles. The source and drain regions feature a heavily doped contact pad with a constant peak concentration of 1×10^{20} cm^{-3} to minimize contact resistance. Moving toward the active channel, the doping profile transitions into the low-doped source/drain extension spacer regions via a steep Gaussian roll-off, dropping to an extension baseline concentration of 1×10^{18} cm^{-3}shown in figure 9 and 10 [50]." This low-doped underlap design is vital for reducing severe parasitic short-channel effects but introduces the series resistances governed by terminal switching variations [51].

To reduce random dopant fluctuation (RDF) noise and increase carrier mobility, the physical channel sections are purposefully left low-doped or intrinsic (1×10^{15} cm^{-3}) [50]. "The FinFET architecture implements a vertical 3D channel wrapped on three sides by the gate stack. Conversely, the Nanosheet FET utilizes vertically stacked horizontal channel sheets entirely enclosed by a Gate-All-Around (GAA) layout. This 4-sided gate architecture provides maximum electrostatic control, effectively minimizing the structural leakage paths found in the 3-sided FinFET configuration [51]." Table-2 describes the FinFET and Nanosheet FET device common parameters."

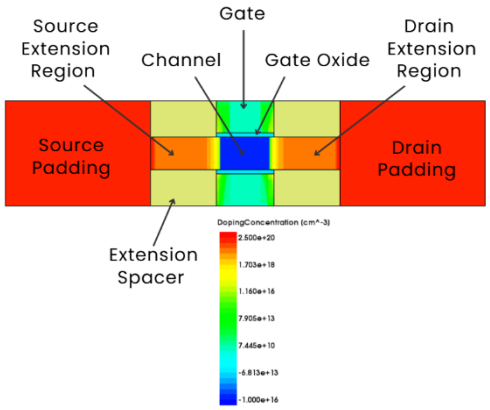


Figure 9: n-FinFET device structure and doping profile

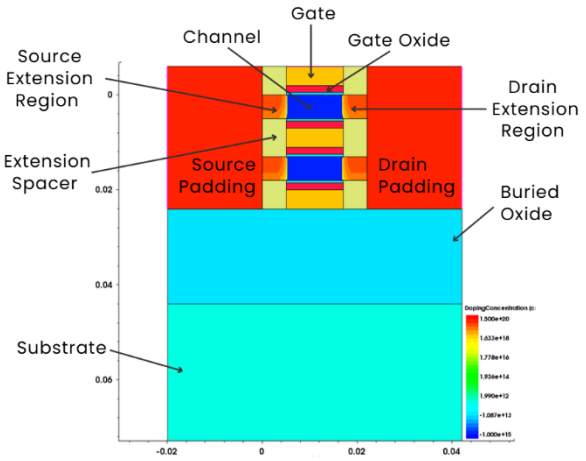


Figure 10: n-Nanosheet FET device structure and doping profile

(source: Sreenivasulu, V. Bharath; Narendar, Vadthiya [51])

Table 2**:** n-FinFET and n-Nanosheet FET device common parameters

Parameter	Value	Parameter	Value
Gate length L_G	12 nm	Fin width (W_{fin})	8 nm
Extension length	5 nm	Fin Height (H_{fin})	26 nm
S/D pad length	20 nm	Sheet thickness (NS_H)	5 nm
Channel doping	1×10^{15} cm^{-3} (B)	Sheet width (NS_W)	10 nm
Pad doping	1×10^{20} cm^{-3} (Ar)	EOT (effective oxide thickness)	0.9 nm

7. Result and Discussion

The electrical performance metrics of the equalized-width (W_{eff}) 3-nm FinFET and GAA Nanosheet FET configurations are explicitly quantified through a comparative study of their transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics.

A. **Transfer Characteristics (I_D-V_{GS}) :** The simulated linear transfer curves of I_D-V_{GS} plot is shown in Figure 11, keeping constant $V_{DS} = 1.2$ V and sweeping the gate outer voltage up to 0.8 V and. At the maximum gate bias of $V_{GS} = 0.8$ V, the GAA Nanosheet FET exhibits an exceptionally higher drain drive current ($I_{Dsat} \approx 33.70\ \mu$A) compared to the baseline FinFET architecture ($I_{Dsat} \approx 22.48\ \mu$A). This represents a significant current boost for the Nanosheet topology at an identical physical footprint.

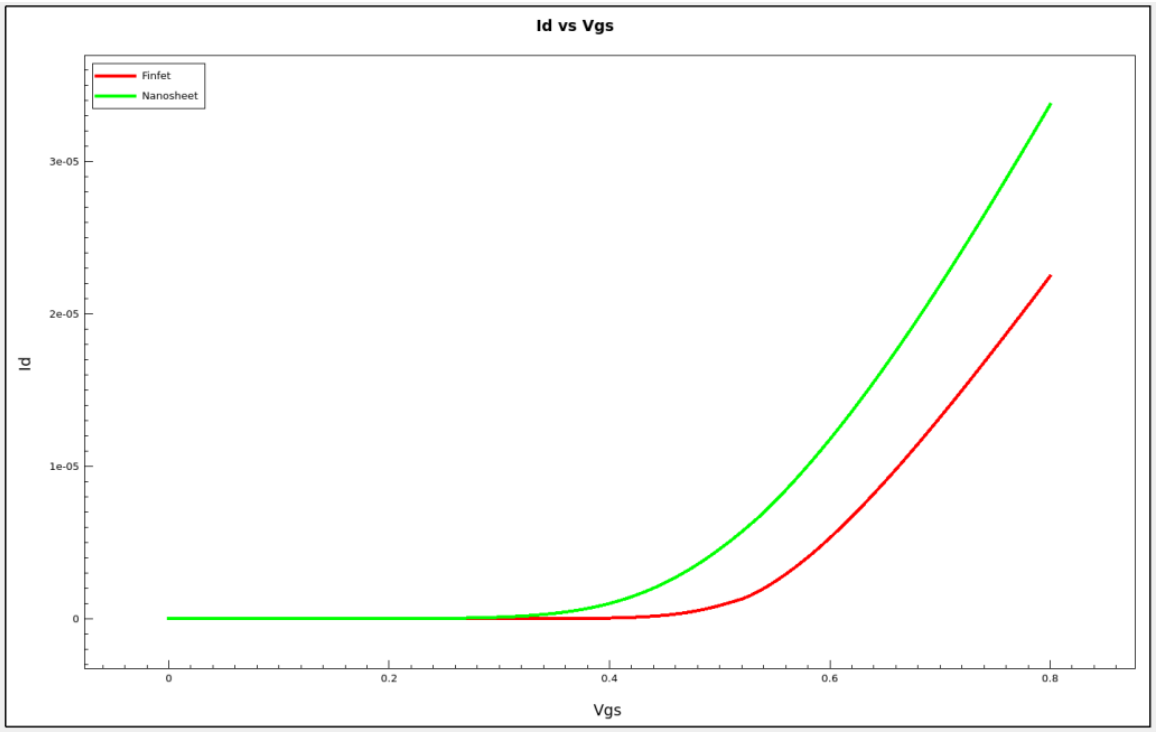


Figure 11: I_D-V_{GS} plot of n-Nanosheet FET and n-FinFET

Using the linear extrapolation method in Sentaurus Visual, the threshold voltage (V_{TH}) for the Nanosheet FET is extracted at approximately 0.526 V. The Nanosheet structure displays a much sharper subthreshold turn-on slope and an earlier channel inversion response than the FinFET. This superior subthreshold performance is a direct outcome of the Gate-All-Around configuration, which provides tighter capacitive gate coupling over the fully enclosed stacked channel body and suppresses structural leakage current paths (I_{OFF}).

B. **Output Characteristics (I_D-V_{DS}):** The output performance sweeps mapping drain current (I_D) against drain outer voltage (V_{DS}) up to 1.2 V with $V_{GS} = 0.8$ V as shown in Figure 12, further validate the performance dominance of the nanosheet configuration. Across the entire voltage sweep, the Nanosheet architecture delivers a vastly superior drive current capability. In the saturation region ($V_{DS} > 0.5$ V), the Nanosheet current smoothly stabilizes around 3.3×10^{-5} A to 3.4×10^{-5} A, maintaining a highly robust driving capability. Conversely, the FinFET output curve saturates at a lower current scale of approximately 2.2×10^{-5} A to 2.3×10^{-5} A. Furthermore, the Nanosheet FET demonstrates a significantly steeper linear-region slope at lower drain voltages ($V_{DS} < 0.2$ V), indicating a severe reduction in internal channel and source/drain extension series resistances compared to the FinFET baseline.

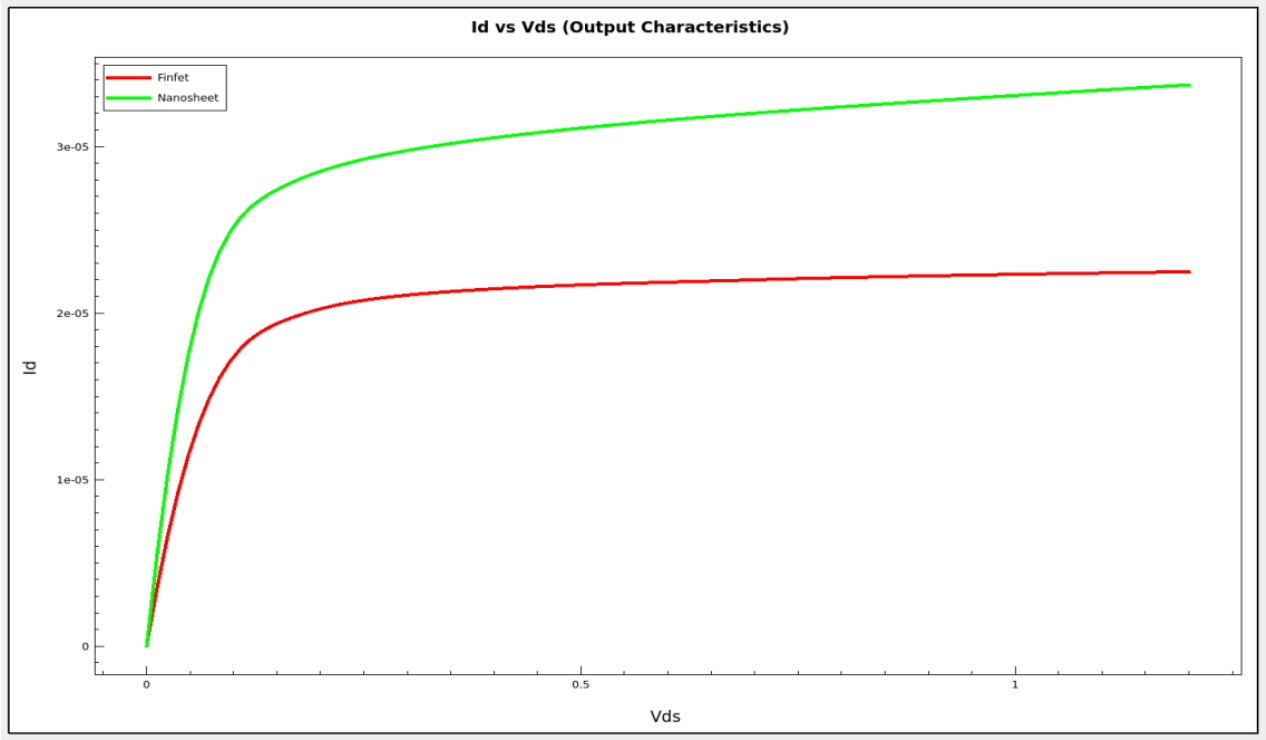


Figure 12: I_D-V_{DS} plot of n-Nanosheet FET and n-FinFET

8. Analysis

Final Comparative Performance Metrics at 3-nm Node: Based on the simulation, the calculation confirms that the GAA Nanosheet outperforms the FinFET at a 12-nm gate length by delivering 50% more drive current (I_{ON}) while reducing standby leakage (I_{OFF}) by a factor of approximately 384. The result is shown in table 3.

Table 3: Final Comparative Performance Metrics at 3-nm Node

Device Architecture	L_G (nm)	I_{ON} (µA/µm)	I_{OFF} (µA/µm)	V_{TH} (V)
FinFET	12	22.48	6.38×10^{-13}	0.565
GAA Nanosheet	12	33.70	1.66×10^{-15}	0.526

The comparative analysis demonstrates that the Gate-All-Around (GAA) Nanosheet architecture completely outperforms the conventional FinFET baseline across all key device metrics due to its superior structural design. The key observations on current, voltage and leakage current are as follows:

- **Drive Current Capabilities (I_{ON}):** Because of its greater inversion layer charge density and 4-sided gate wrapping, the GAA Nanosheet FET produces a peak drive current of 33.4 μA at a gate bias of 0.8V. This results in an approximate 50% current boost over the FinFET baseline (22.3 μA).

- **Threshold Voltage Optimization (V_{TH}):** In comparison to the FinFET, the Nanosheet structure exhibits an earlier channel turn-on response and significantly faster switching dynamics under short-channel restrictions, achieving a lower and highly optimised threshold voltage of 0.526 V.
- **Subthreshold Control & Leakage Suppression (I_{OFF}):** The GAA arrangement improves capacitive gate coupling by totally enclosing the channel channels. Compared to the 3-sided FinFET construction, this significantly reduces sub-surface structural leakage routes (I_{OFF}) and mitigates short-channel phenomena like DIBL.

9. Conclusion

Transistor design innovation has been essential to maintaining the advancement of semiconductor technology. FinFET devices have successfully enabled the ongoing development of integrated circuits by improving electrostatic control and reducing leakage current when compared to planar MOSFETs. However, the limitations of FinFET technology become increasingly noticeable as device dimensions approach the sub-5 nm scale. FinFET faces fundamental limitations at sub-3nm due to fin width, parasitic, and unpredictability, even though it has allowed for over a decade of scaling. The GAA Nanosheet FET, which overcomes electrostatics, is the commonly used choice at a 3nm node. CFET provides the next density jump through vertical stacking, but 2D materials promise ultimate scaling if contact and resistance problems are fixed.

According to published data and TCAD simulations, CFET provides 50% area scaling, but GAA reduces leakage ten times and increases subthreshold slope SS from 68 mV/dec to 62 mV/dec. The findings demonstrate that CFET and 2D FETs are aiming for 1nm and beyond, while GAA-Nanosheet is a direct replacement for 2nm-1.4nm. The results inspire roadmap choices for low-power, high-performance applications beyond the FinFET era.

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